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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re application of Tetsuya AKIMOTO, et al.

Docket No: Q55026

Appln. No.: 09/347,409

Group Art Unit: 2123

Technology Center 2100

Confirmation No.: 3821

Examiner: DAY, HERNG-DER

Filed: July 06, 1999

For: METHOD AND COMPUTER SOFTWARE PRODUCT FOR CALCULATING AND PRESENTING A NUMERICAL VALUE REPRESENTATIVE OF A PROPERTY OF A CIRCUIT (As Amended)

AMENDMENT UNDER 37 C.F.R. § 1.116

ATTN: BOX AF  
Commissioner for Patents  
Washington, D.C. 20231

Sir:

This preliminary amendment, responsive to the Office Action dated December 19, 2002, is being filed as part of a Continued Prosecution Application. Please amend the above-identified Application as indicated below. An enclosed Appendix contains the amendments with markings to show changes made.

IN THE SPECIFICATION:

Paragraph bridging pages 3 and 4:

According to this invention, a method for calculating pin-to-pin delay time  $T_{iopath\_aged}$  and block-to-block delay time  $T_{connect\_aged}$  is provided. The pin-to-pin delay time  $T_{iopath\_aged}$  is delay time of a signal passing between an input pin and an output pin of a logic block. The block-to-block delay time  $T_{connect\_aged}$  is delay time of a signal passing between said two logic blocks connected to each other in a computer. Furthermore, this method comprises the following steps:

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